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APPLICANT
Alok Jain, et al.

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U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	PATENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE

FOREIGN PATENT DOCUMENTS

EXAMINER'S INITIALS	PATENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
						Yes	No

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

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WP	R. Razdan, et al., "Clock Suppression Techniques for Synchronous Circuits," IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems, pp. 1547-1556, October 1993.
WP	F. Rocheteau, et al., "Tralala: A Fast and Accurate Functional Abstraction Tool For Transistor Netlists," SAME 99, Accessible from http://www.sansistor.com .
WP	"Statement of Product Sale," 8 pages, December 1999.
EXAMINER <i>[Signature]</i>	DATE CONSIDERED <i>7/2004</i>

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.